# Abhijit Dutta

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## PROFESSIONAL SUMMARY

I align myself to the Vision of the Company and Greater Good positioning myself so as to be best suited for the trouble in town and deal with it. I am the guy you call up the last minute your impossible looking mission meant for the greater good goes south.
Staff R&D Engineer with nearly 8 years in Electronic Design Automation specializing in compiler infrastructure, hardware-assisted verification, and FPGA prototyping. Proven record of delivering high-impact solutions for tier-1 semiconductor customers, leading cross-BU initiatives, and owning key product components at Synopsys and Infineon. Skilled in architectural design, customer escalation handling, and mentoring senior engineers across global teams.

## TECHNICAL SKILLS

### LANGUAGES
Prompt Engineering
C • C++ • C# • TCL
SystemVerilog • VHDL
Testbenches • UPF •SDC
TypeScript • CSH Scripting
Java • JavaScript • SQL
Python• Solidity • Assembly

### TOOLS & FRAMEWORKS
VIM • GDB • Lex-Yacc
VS Code • Rider• Copilot
Google Test • Coverity
Maketools • Git • Perforce • Blazor
Django • Nginx • Gunicorn
PostgreSQL • Oracle • AWS EC2
Node JS • Rest API

### INDUSTRY EXPERTISE
Synthesis based Compiler
Simulation, Prototyping & Emulation
Formal Verification • Static Analysis
RTL Code Gen • Tech Mapping
Encryption (AES / RSA)
RAG based Generative AI
Blockchain
Full stack development

## WORK EXPERIENCE

### INFINEON TECHNOLOGIES | Staff Engineer, R&D
Sept 2025 – Present | Bengaluru, India

- Leading operation for on-boarding multiple internal legacy customers on our Platform based Design Automation tool.
- Building a Common Plug-and-Play Platform for scalable IP development across the organization.
- Applying CAD methodologies for pre-RTL code generation and collateral generation workflows.
- Developed C# / Blazor-based GUI for form pages and an NLView-based schematic viewer.
- Implemented VS Code extension UI enhancements using TypeScript.
- Integrated Generative AI agents and RAG architecture into development workflows.
- Leading university hiring initiative through a company-wide Hackathon program.

### SYNOPSYS INC. | Staff Engineer, R&D
June 2018 – August 2025 | Bengaluru, India

- Developed end-to-end features across a Mixed-Language (SystemVerilog / VHDL) Compiler — from Lex-Yacc parser through Elaboration, Word-Level Synthesis, Tech Mapping, and Netlist generation.
- Provided architectural guidance to senior R&D engineers and managers across multiple business units and international geographies.
- Delivered compile-time optimizations and critical feature releases for major semiconductor customers with direct client interaction.
- Owned key components of industry-leading products: ZeBu, Synplify, HAPS, VC Static/Formal.
- Recognized for high-impact technical presentations in company-wide forums.

Key Contributions:

- Drove productization of Hardware-Assisted Verification (Emulation & Prototyping Continuum).
- Designed and implemented encryption support (AES/RSA) for HAPS product line.
- Architected Modular Compile for HAPS, including cross-module reference (XMR) resolution.
- Owned DesignWare IP integration for the Hardware-Assisted Verification platform.
- Served as VCS Parser Expert (Lex/Yacc-based front-end).
- Led Distributed Scaling architecture for the compiler back-end.
- Owned RTL construct implementation across HAV products: XMR, Interfaces, Pragmas, Encryption, Task/Function, Readmem.
- Supported ZeBu Transactors for the Unified Compiler platform.
- Ideated XMR and UPF solutions for the Distributed Unified Compiler.

## EARLY CAREER

### HASHCASH CONSULTANTS | Software Engineering Intern
May 2017 – June 2017 | Kolkata

- Built a Blockchain DApp on Ethereum with Smart Contracts for decentralized data transfer.
- Developed a Spring MVC web app connecting to the Stellar Federation Server.

### BEATEST.IN | Software Engineering Intern
Feb 2017 – Mar 2017 | Remote

- Deployed a production LEMP stack (Linux, Nginx, MySQL, PHP) on AWS EC2 for a WordPress site.

### I.T.R.A. HEALTH REMOTE PROGRAM | Research Intern
May 2016 – July 2016 | Jadavpur University, Kolkata

- Developed a JSP Servlet web application enabling remote doctor-patient prescription review.

## EDUCATION

### JADAVPUR UNIVERSITY
B.E. in Computer Science
May 2018 | Kolkata
Cum. GPA: 7.73 / 10

### JAWAHAR VIDYA MANDIR
C.B.S.E.
May 2013 | Ranchi
Percentage: 88.4%

### ST. THOMAS SCHOOL
I.C.S.E.
May 2011 | Ranchi
Percentage: 93.85%

## RESEARCH & ACADEMIC PROJECTS

### ASSOCIATION RULE MINING | Research Scholar
Identified low-support, high-confidence gene patterns under Prof. Ujjwal Maulik, Head of Dept.

### LEXICAL ANALYSER & LL(1) PARSER
Built a C-language lexical analyzer and predictive parser from scratch.

### SIC ASSEMBLER
Implemented a two-pass SIC assembler for machine code generation.

### MACHINE LEARNING
Implemented Fuzzy K-Means clustering and Fuzzy KNN classifier; benchmarked on standard datasets.

## COURSEWORK

Cryptography • Compiler Design • Data Structures & Algorithms • Operating Systems • Database Management • Object-Oriented Programming

## INTERESTS

Electronic Design Automation • Information Security • Full Stack Development • Competitive Programming • Generative AI • IoT